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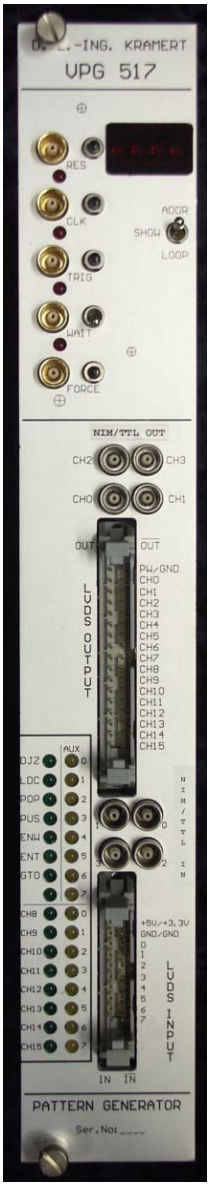


INSTRUCTION MANUAL

CLOCKED PATTERN GENERATOR

VPG 517 REV: E

All technical data subject to change without notice.

January 2003

Preface:

- The main changes of this "revision E" are:
  1. "Force-Input" : bug removed
  2. LEMO inputs and outputs can now drive and receive TTL- and NIM-level signals.
  3. New multilayer mainboard to improve noise margins.

- We have replaced some designators with more catching expressions. As an example the old name of S6/D3 bit was **"Enable internal clock"**. The new expression is " **Internal CLOCK ON/OFF (1=ON)**". All bits kept their old function. This version of the VPG517 has been tested by PSI with the same pixel detector readout environment and programs as its VPG517 predecessor without any problems.

- The term "**JUMP**"-Input has been replaced with the new term "**TRIG**"-Input because it describes better the function of this input. In the compiler software und on some other places the old term "**JUMP**" may still appear.

- Because the VME-RAM is 4 byte wide, the address by the PC interface is **four** times the VME-address. If not specified otherwise, we use the PC interface address.

Description:

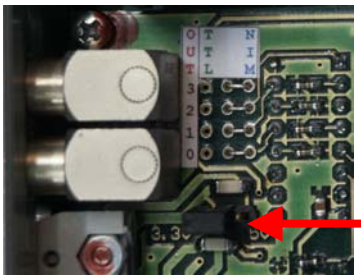
This Pattern Generator has a DSP-like structure. All commands are executed within one clock cycle. A command word consists of 32 bit. The memory is 32 bits wide and each address contains a command-word. 16 bit pattern, 8 bit MSB-address and 7 bit commands and flags. Within each clock cycle the command bits are interpreted and executed. After reset the address counter starts with address 0x0000. Without a command bit set, the address counter increments with each clock and the 16 bit pattern are sent to the LVDS- and TTL/NIM-output ports. With the PUSH bit (D4) set, the 15-bit address counter content is pushed to the stack and loaded with the subroutine address from the command word D15..D8.The least significant bits of the address counter are cleared. See index d) for details. Like a DSP the program continues until it recognizes a POP-bit (D3) set. Then the address-counter is loaded from the stack and incremented. The stack has a depth of two, so you can even execute a subroutine within a subroutine. Another nice feature is the 8 bit loop-counter. Decrementing the loop-counter, compare with zero and conditional jump is done within the same single clock.
Minimum pattern-pulse width is 25ns. This is realized with an internal Clock of 80 MHz (location see picture 2) and the clock divider set to 1 (formula see index j).

Main Features of the Pattern Generator are:

a) 16 Bit Pattern LVDS, TTL or NIM D31..D16 (VME-Bus)
b) 32 K x 32 Bit RAM
c) 2 Stacks
d) 1 Goto-Command (even boarders = 128 Bytes) MSB-Byte D15..D8 (VME-Bus)
e) 1 Loop Counter (max. 255 counts)
f) 1 Wait LEMO Input TTL
g) 1 TRIG LEMO Input TTL (old "Jump")
h) Memory directly readable and writeable from VME-Bus (D31..D0) 32 bit access
i) Pattern Generator Address Counter
j) Internal Clock- Generator with programmable clock divider (1,2,3,..15)
k) Force Input TTL jumps to 0x1FE00 and from here with goto to somewere else
l) 8 x LVDS Inputs, readable via status-register S1, 0x1FFE8
m) Pulse-delay for CH14,15. Programmable in 1 ns steps (max. 255 ns) via status-register 0x1FFEC
n) "OR"-gates with output-pattern, programmable via status-register S6 (0x1FFFC) or S0 (0x1FFE4)
o) Invert DIP-Switch to invert the LVDS- INPUTS and OUTPUTS

to a)
The upper 2 Bytes of the VME-Bus contain the Pattern and are accessible from the front panel

- via edge connectors CH0..CH15; 16 Bit LVDS Outputs
- via LEMO CH0..CH3; either TTL or NIM level into 50 Ohm



Plug the jumper to the appropriate level.
NIM outputs are **current** outputs! They need the 50 Ohm termination on the end of the line for proper levels.

Power-Selector for LVDS-OUTPUT connector. Supplies 3.3V/1A or 5V/1A to connector pin34. This power is secured with the adjacent 1A SMD-

Picture 1: LEMO Output Level selector

to b)
Memory 32K x 32 Bit (8 ns)
The whole memory is directly readable and writeable from the VME-Bus (transparent) (refer to point h).
The memories are **not** dual ported rams. Therefore VME-access to the memories interrupts the pattern, except access via the bypass S0 (0x1FFE4) and S1 (0x1FFE8).

to c)
2 Stacks for sub routine calls.
With the PUSH-Command (Bit D4) the actual RAM-address (15 bit) is pushed to the Stack and the RAM-Address-Counter is loaded with the 8 Bit MSB-address of the subroutine. The 7 LSB-Bits are cleared. Make sure that your subroutines start at 128 bit boarder.
With the POP-Command (bit D3) the RAM-Address-Counter will be loaded with the incremented address from the stack. Two levels are available, that means you can do a subroutine call in a subroutine and pop two levels back to your main program.

to d)
Goto Command (Bit D7): Similar to the Push-Command, you can jump to the 128 bit boarders within the RAM without pushing your actual address to the Stack.

RAM	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
Goto ADR:	D15	D14	D13	D12	D11	D10	D9	D8	0	0	0	0	0	0	0

The Goto address is on the RAM databus D15..D8. The command is activated by setting the data bit D7. The compiler has to take care that labels are always located on RAM addresses with the last 7 LSB Bits = 0.

	PC-address	VME-address
Examples:	0x00200	0x0080 = 128
or:	0x00400	0x0100 = 256

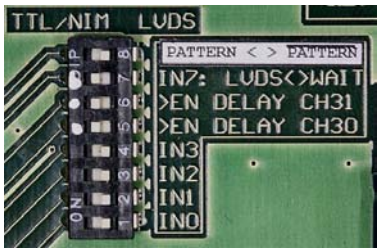
By doing so you waste some memory but you get 7 data bits free for additional features. The memory has been increased from 2K to 32K so the loss of memory is negligible. In a program with 10 labels you are losing max. 1,28 KByte.

to e)
Loop Counter (D2): An 8-Bit Loop Counter can be loaded through the RAM-Address-Bus (D15..D8). With the DECJZ-Command (Decrement, Jump If Zero) (D1) the Loop Counter is decremented. If the Loop Counter is zero, the Address-Counter skips the next address. This enables program branches.

Example:		Pattern	LDCTR 100
	Label:	0 1 0 1 0 0 ;	
		1 1 0 0 1 1 ;	
		0 0 1 0 0 1 ;	DECJZ
		0 0 1 0 0 1 ;	GOTO LABEL
		0 0 0 1 1 1 ;	

to f)

Wait: There is a Wait Enable-Bit D5. If this Bit is set, the address counter waits until the Wait/Go Input (front panel) is high or a VME-GOTO command is executed. That means that the program runs to this point and waits for the /WAIT signal before continuing. You can read this bit via bypass-statusregister S1(0x1FFE8)/Bit7. By polling this register you get to know wether the address counter already reached the address with the wait-bit set. You can select with Dip-Switch 7 between LVDS Input D7 and /WAIT Bit-D5 (RAM).



Dip-Switch 7	
ON (default)	OFF
LVDS-IN7	/WAIT D5

Picture 2: VPG-IO Board DIP-SWITCH

to g)

Jump: Similar to the Wait function, there is a Jump LEMO Input on the front panel as well as an EN Jump Bit (D6). If the Jump Input is enabled (D6 = 1), and the jump signal on the LEMO input is high, then the address counter skips the next address and jumps to the next following address. This enables program branches.

```
Example:                Pattern
              M1:       0 1 0 1 0 0 ;
                        1 1 0 0 1 1 ;       EN_JMP
                        0 0 1 0 0 1 ;       GOTO M1
                        0 0 1 0 0 1 ;
                        0 0 0 1 1 1 ;
```

If a Jump signal is on the LEMO input, the address counter skips the next address.

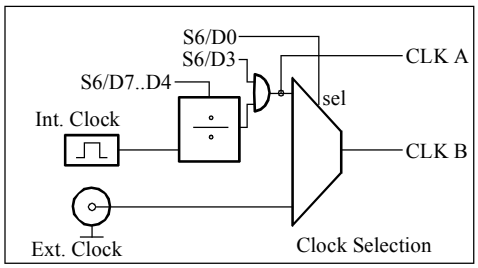
to h)

Pattern Generator Ram read and write via VME-BUS. The address range is selected by a 2x8 Bit-Dip switch (address selector, A31..A17). This address range is accessible via read and write commands (A32, D32; or A24, D32). The extended address range is selected via jumper SW2/1 S/E (see Picture 10). When reading and writing via Status comands S2..S6 the Pattern Generator Address Counter is automatically removed from the address bus and after the VME-access connected again.

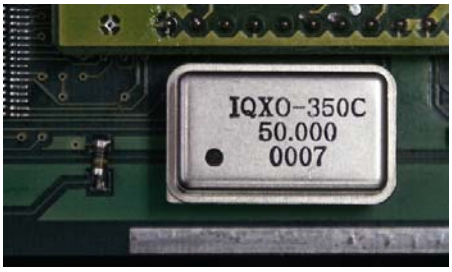
to i)

This Pattern Generator is equipped with a fast 15 Bit address counter. The address counter is incremented with each clock either from the front panel or from the VME side. The address counter can be loaded with 8 MSB Bits. The lower 7 LSB Bits are cleared. As described under e) and g), the address counter is able to increment 2 for program branches.

to j)
On board pluged quarz oszillator. This quarz oszillator can be selected as the source for the clock input.
It is switched ON/OFF with bit S6/D3 in the status register. The intern/extern clock select bit S6/ needs to be set for internal clock. Clock-division factor is programmed with status bits D7..D4. This divider works only with the internal clock source. Pattern-pulse-width = $1/f_{quarz}*(n+1)$ with n=1,2,3,..15

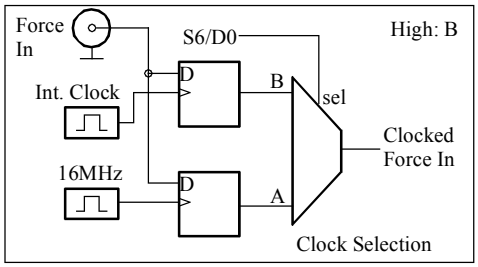


Picture 3: Clock divider and selection



Picture 4: Int. Clock socket

to k)
With "Force" input high the address-counter jumps to 0x7F80 (0x1FE00 PC-Interface). The input is synchronized either with the CLK-A (S6/D0=1) or with the 16 MHz system clock (S6/D0=0).
Force input can be disabled with S6/D0=1 and S6/D3=0.

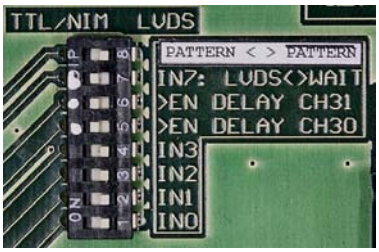


Picture 5: Clocked Force input

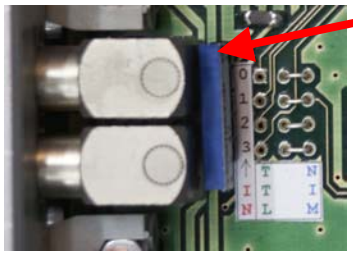
to l)
This inputs are either

- 8 Bit LVDS inputs
- 7 Bit LVDS inputs CH0..CH6 and one /Wait RAM-Bit (D5 of the actual RAM-address) on CH7

Each of the **lower four** input bits can be selected with individual input levels: LVDS, TTL or NIM.



Picture 6: VPG-IO Board DIP-SWITCH

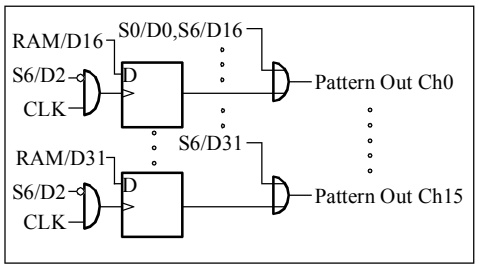


Picture 7: TTL/NIM-Input selector

With Dip-Switch 1..4 "OFF" LVDS level is selected. Input source is the 20-pin LVDS-INPUT connector.
With the switch "ON", either TTL or NIM level is selected. Now the input source is the LEMO connector. All combinations are allowed, **but no hardware protection** is made if NIM-level signals are fed to a TTL input and vice versa. The TTL-inputs are terminated with a resistor pack of 4x 50 Ohm. If needed this can be replaced by a resistor pack of 4x1kOhm. The NIM-inputs termination is 50 Ohm and not affected by the TTL-input termination.
This inputs are readable via bypass status register S1 (0x1FFE8).

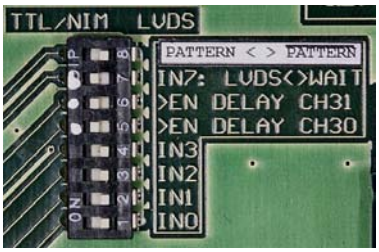
to m)
This function delays Pattern CH14,CH15. The delay is programmable in 1ns steps via delay-register 0x1FFEC.
CH 15 : D7..D0;
CH 14 : D15..D8;
There is an inner delay of 10ns, when feeding this signals through the delay chips. If the delay function is not needed, you can switch the signals directly to the output which avoids this inner 10ns delay (DIP-SW5,6 "ON").

to n)
This "OR"-gates are bitwise ORed with the Output-Pattern. They are writeable via the status register S6 (0x1FFFC) bit D31..D16. Or CH7..CH0 also via bypass status register S0 (0x1FFE4) bit D7..D0.



Picture 8: ORed Pattern

to o)



Picture 9: VPG-IO Board DIP-SWITCH

The default position of SW8 is "OFF". This is the compatible position to the predecessors. With this switch the LVDS- inputs and outputs will change polarity. E.g Q became /Q and vice versa.

VME Interface

The RAM of the Pattern Generator is located between 0x0000..0x7FF0 (32K x 4Byte width) or from PC interface 0x00000 .. 0x1FFFF (128K x 1Byte width).

Access via A24D32 (standard) or
A32D32 (extended) (Dip Switches on Pattern Generator)
For description of the Dip Switches refer to page 10.

STATUS [S0] address: 0x1FFE4 (write only)
Action: Write 8 bit data to the output "**OR**" register
Databus: D7..D0 output data
This port is independently accessible **without disturbing the pattern generator output and speed (bypass).** The „"OR"-register byte is ORed with the pattern-generator output pattern CH7..CH0.
The function of this command is the same as writing to statusregister **[S6]** 0x1FFFC D31..D16, except the fact that the pattern generator function is not interrupted. This command writes exactly to the same "OR" gates and the datas are readable via statusregister **[S6]** 0x1FFFC D23..D16

STATUS [S1] address: 0x1FFE8 (read only)

Action: Read 8 bit LVDS-Inputs or, at D7 the /WAIT-Bit or LEMO inputs

Databus: D7..D0 is the Input byte

This port is independently accessible **without disturbing the pattern generator output pattern or speed (bypass).**

The function of this command is the same as reading from statusregister **[S6]** 0x1FFFC D15..D8, except the fact that the pattern generator function is not interrupted.

STATUS [S2] address: 0x1FFEC (write only)

Action: Load the Delay Register with new delays.

Databus: D15..D8 is the delay in ns for Pattern Bit 15

D7..D0 is the delay in ns for Pattern Bit 16

STATUS [S3] address: 0x1FFF0 (write only)

Action: Load the PG address counter with a new address.

Databus: D15..D8 is put to the 8 MSB Bits of the address counter. The lower LSB Bits are cleared.

- Enable VMECLK-Bit has to be set in statusregister **[S6]** 0x1FFFC-Bit 0
- Goto-Bit (D7) must be set
- D0..D6 must be cleared

STATUS [S4] address: 0x1FFF4 (write only)

Action: PG address counter is cleared.

Databus: No data needed (dummy datas)

STATUS [S5] address: 0x1FFF8 (write only)

Action: Single Clock to the Pattern Generator address counter.

- EN_VMECLK-Bit has to be set in statusregister **[S6]** 0x1FFFC – Bit 0

Databus: No data needed (dummy datas)

STATUS [S6] address: 0x1FFFC (write)

Action: Overwrite the three status bits

Databus: D0: INT/EXT Clock (1=INT) (Enable VME CLOCK, **must be 1 if int. clock is used (D3))**

D1: Tristate PG-Address-Counter

D2: Freeze Output-Pattern (see picture 8)

D3: **Internal** CLOCK ON/OFF (1=ON)

D4 Internal Clock-Divider LSB

D5 Internal Clock-Divider

D6 Internal Clock-Divider

D7 Internal Clock-Divider MSB

D15..D8 : not used for "write"

D31..D16 “OR“- Register

STATUS [S6] address: 0x1FFFC (read)

Action: Read the status bits:

Databus: D0: INT/EXT Clock (1=INT) (Enable VME CLOCK)

D1: Tristate PG-Address-Counter

D2: Freeze Output-Pattern (see picture 8)

D3: **Internal** CLOCK ON/OFF (1=ON)

D4 Internal Clock-Divider LSB

D5 Internal Clock-Divider

D6 Internal Clock-Divider

D7 Internal Clock-Divider MSB

D15..D8 : External LVDS- or LEMO Inputs

D31..D16 “OR“- Register

Pattern-RAM : 0x00000 ..0x 1FDFC
Bit Assignment:

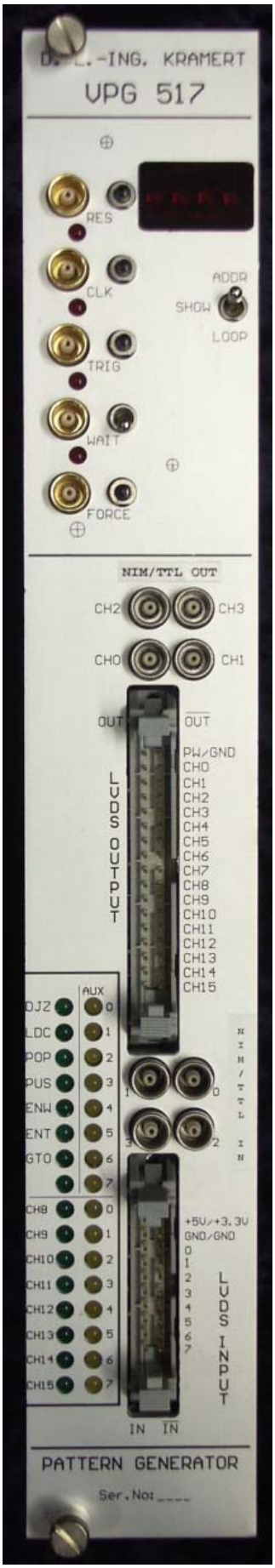
D31..D16	Pattern (16 Bit)
D15..D8 (AUX7..0)	- Jump Address - Load data for Loop-Counter - Subroutine Jump-Address
D7	PG-Goto Bit
D6	Enable Jump
D5	Enable Wait (readable via bypass register S1/D7)
D4	PG-Push
D3	PG-Pop
D2	Load Loop Counter
D1	Decrement Loop Counter, jump if Zero
D0	not used

Address Assignment: (PC-INTERFACE 128K x 1BYTE)

0x00000..0x1FDFC	Pattern-RAM
0x1FE00	"FORCE" jump address
0x1FFE4	[S0] Bypass Write - D7..D0 "OR" to LVDS output CH7..CH0
0x1FFE8	[S1] Bypass Read - D7..D0 LVDS input CH7..CH0
0x1FFEC	[S2] Delay-Register
0x1FFF0	[S3] Status Write: Load PG-Address-Counter with D15..D8, LSB-Bytes become 0 - D7 Goto Bit must be set - D0..D6 Bits must be cleared
0x1FFF4	[S4] Status Write: Reset PG-Address-Counter
0x1FFF8	[S5] Status Write: Clock to Pattern Generator - EN_VMECLK-Bit has to be set in statusregister **[S6]** 0x1FFFC – Bit 0
0x1FFFC	[S6] Status Bits Read or Write: - D0 INT/EXT Clock (1=INT) (Enable VME CLOCK) - D1 Tristate PG-Address-Counter - D2 Freeze Output-Pattern (see picture 8) - D3 Enable Internal Quarz Oszillator - D4 Internal Clock-Divider LSB - D5 Internal Clock-Divider - D6 Internal Clock-Divider - D7 Internal Clock-Divider MSB - D15..D8 External LVDS/LEMO-Inputs - D31..D16 “OR“- Register

The base address can be mapped with the Dip Switches to 128K boarders .

Front Panel Connectors



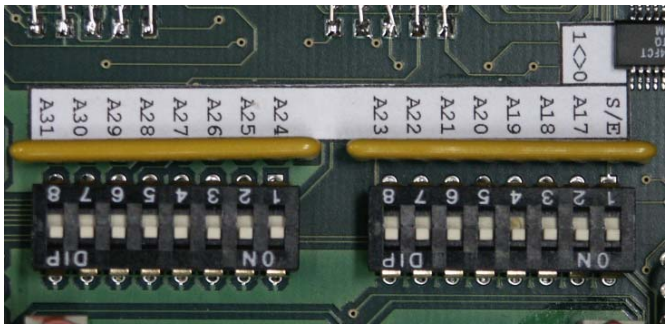
OUT Ch15..Ch0	Edge connector, signal out in LVDS-Logic. All output channels have LED's.
OUT Ch3..Ch0	Lemo Connector high active, signal out in **TTL logic** "0" < 0.5 V; "1" > 2.4 V across 50 Ohm to ground low active, signal out in **NIM logic** "0" 0 V; "1" – 0.7 V across 50 Ohm to ground
IN Ch7..Ch0:	Edge connector, signal in LVDS-Logic.
IN Ch3..Ch0:	Lemo Connector **TTL** "0" <0,8V, "1" >2V high active, signal: impedance 50 Ohm **NIM** "0" 0V, "1" -0.7V low active, signal: impedance 50 Ohm
RES	Lemo Connector Low active, signal: impedance 1KOhm TTL "0" <0,8V, "1" >2V, pulse width min. 20 ns
RES-PUSH Button	Press button for reset.
CLK	Lemo Connector. High active, signal: impedance 1KOhm TTL "0" <0,8V, "1" >2V, pulse width min. 25 ns Max. clock frequency typ. 40 MHz.
CLK PUSH Button	Press button for one clock pulse.
TRIG (JMP)	Lemo Connector High active, signal: impedance 1KOhm TTL "0" <0,8V, "1" >2V
WAIT/GO	Lemo Connector High active, signal: impedance 1KOhm TTL "0" <0,8V, "1" >2V
FORCE-IN	Lemo Connector High active, signal: impedance 1KOhm TTL "0" <0,8V, "1" >2V
Display	
4 Digit hex	With the SHOW switch in the ADDR-Position the display shows the 15Bit-Pattern-Generator Address-Counter. With the SHOW switch in the LOOP-Counter-Position the display shows the 8Bit-Loop-Counter.
LED AUX0..7	Shows: • With Goto-Command: MSB-Jump-Address • With Load-Command: LOAD Data for Loop Counter • With Push Command: Subroutine Jump Address
GTO LED	Goto Command is executed with the next clock.
ENJ LED	Enable-Jump Led: When on, the Jump-Input is enabled.
ENW LED	Enable Wait. When on, Wait-Input is enabled.
PUS LED	PUSH-Command is executed with the next clock. Jumps to the address shown in D8..D15 LED's.
POP LED	POP-Command is executed with the next clock.
LDC LED	Load Loop Counter Loop-Counter is loaded with the Data shown in AUX0..7 Led's, with the next clock.
DJZ LED	Decrement Jump if Zero is executed with the next clock

Picture 10: Front Panel

Dip Switch Settings

Address Decoder:
The STA/EXT switch is the first Dip Switch. Standard address range (A23..A2) is selected with the switch in **OFF**-position. The extended address switches A31..A24 are then disabled.

Base address (**PC-Interface**):		A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	**A24/ A32**
with the STA/EXT-Switch = OFF:																	
Decimal	hexadecimal																
0	0x000000	x	x	x	x	x	x	x	x	ON	ON	ON	ON	ON	ON	ON	**OFF**
131072	0x020000	x	x	x	x	x	x	x	x	ON	ON	ON	ON	ON	ON	**OFF**	**OFF**
162144	0x040000	x	x	x	x	x	x	x	x	ON	ON	ON	ON	ON	**OFF**	ON	**OFF**
524288	0x080000	x	x	x	x	x	x	x	x	ON	ON	ON	ON	ON	**OFF**	**OFF**	**OFF**
with the STA/EXT-Switch = ON:																	
0	0x00000000	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	**ON**
131072	0x00020000	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	**OFF**	**ON**
162144	0x00040000	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	**OFF**	ON	**ON**
a.s.o.																	



Picture 11: Base Address DIP-SWITCHES

When all switches in ON-position (default), then Base address : 0x0, extended address range selected

Address Modifier:

	Addressing Space	AM-Codes
STA	STANDARD A2..A23	3D, 39
EXT	EXTENDED A2..A31	0D, 09

Temperature Range: Ventilated VME-Crate is required.
Power Requirements: approx. 1 A at +5V
Physical: Double width VME module